

AUS920010610US1

Sawada

Hardware Validation Through Binary Decision
Diagrams Including Functions and Equalities

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FIG. 1

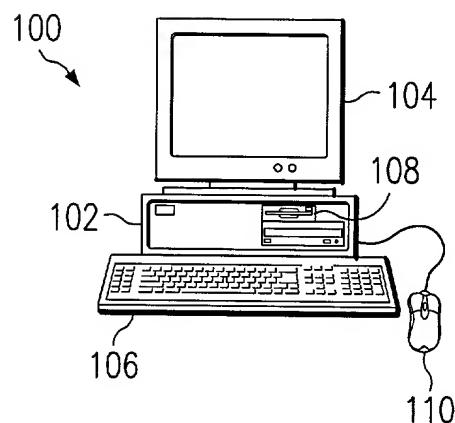


FIG. 2

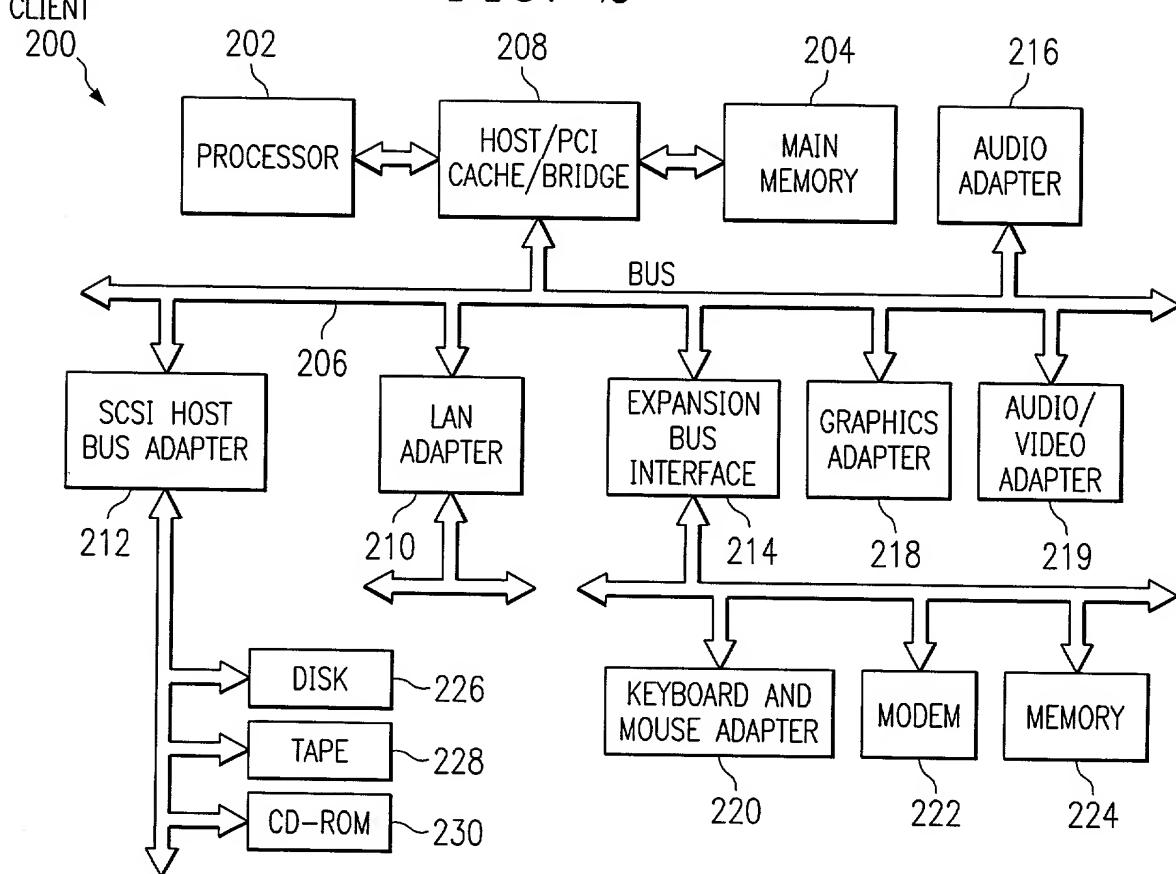


FIG. 3

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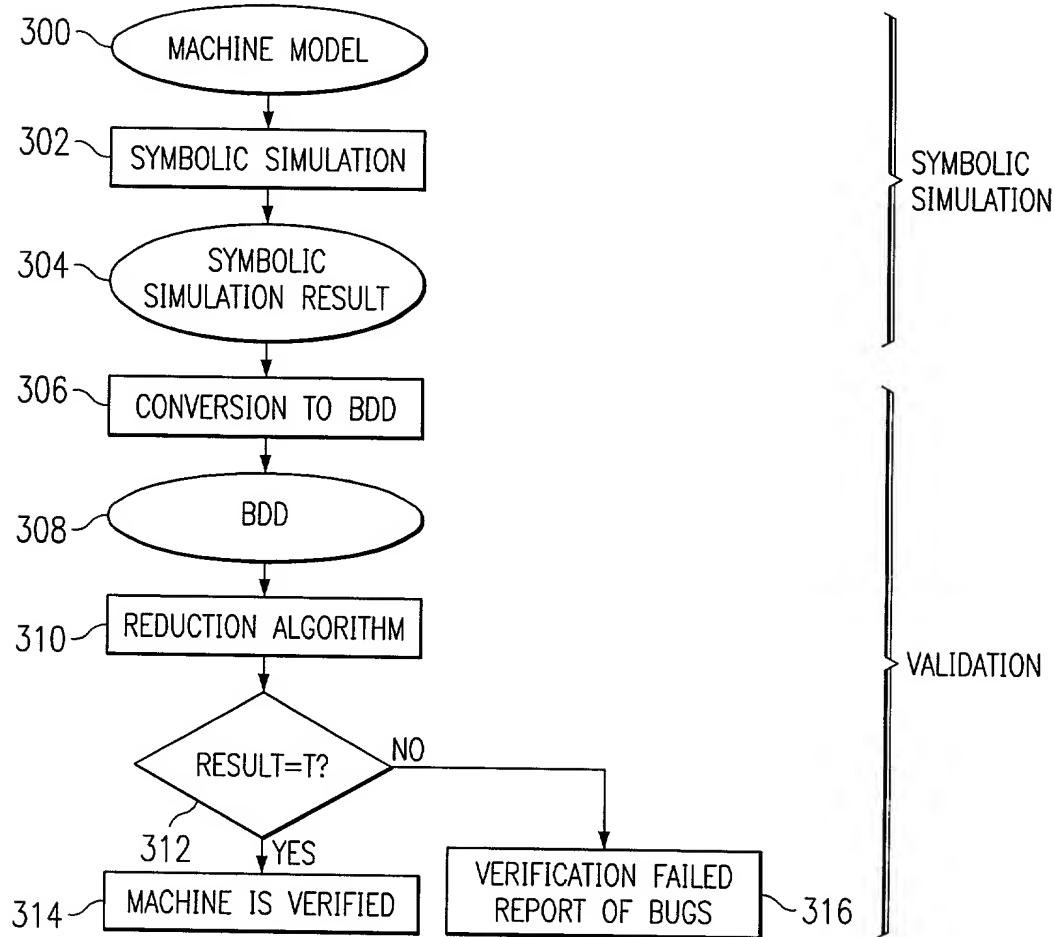
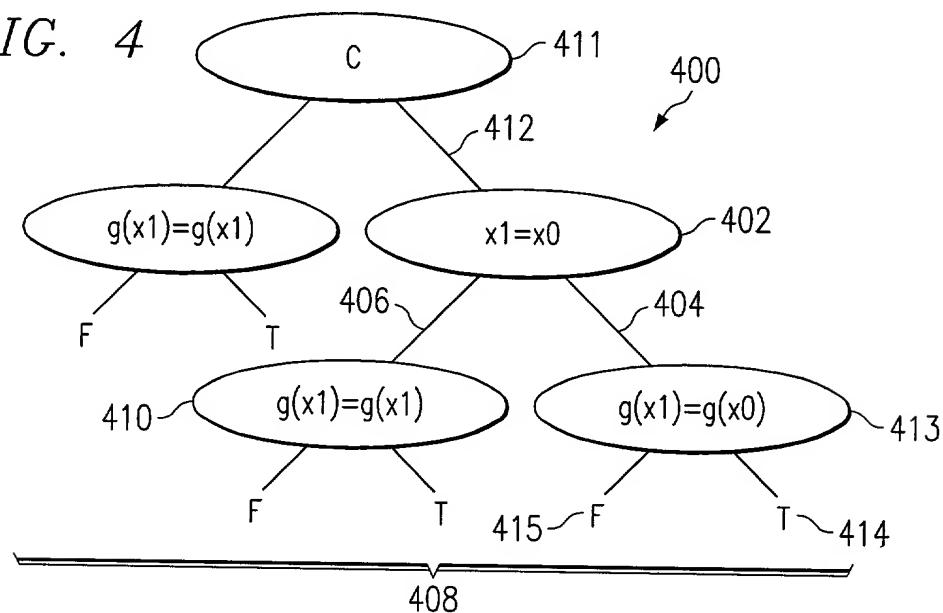


FIG. 4



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FIG. 5

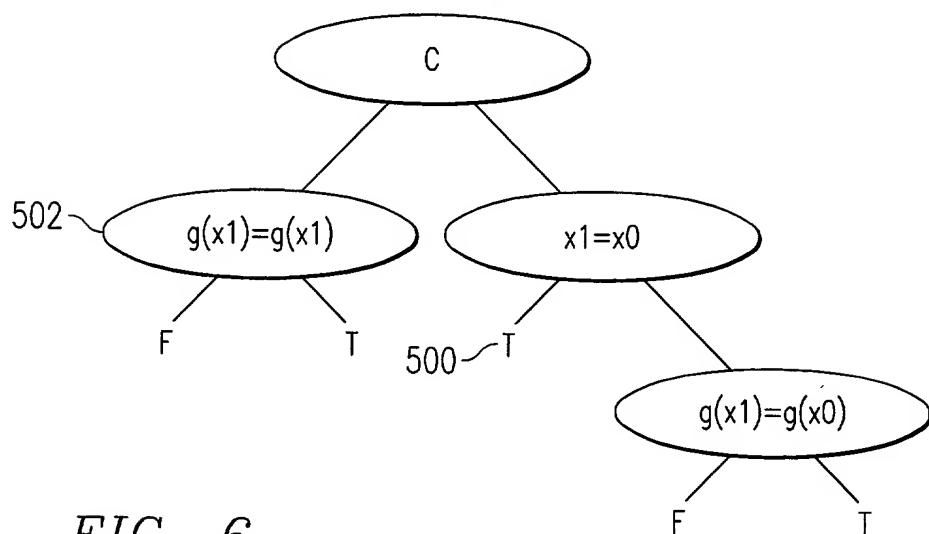


FIG. 6

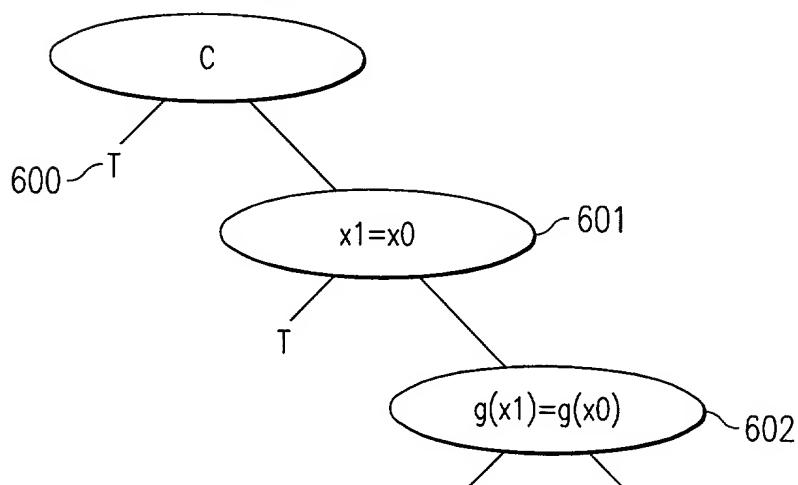
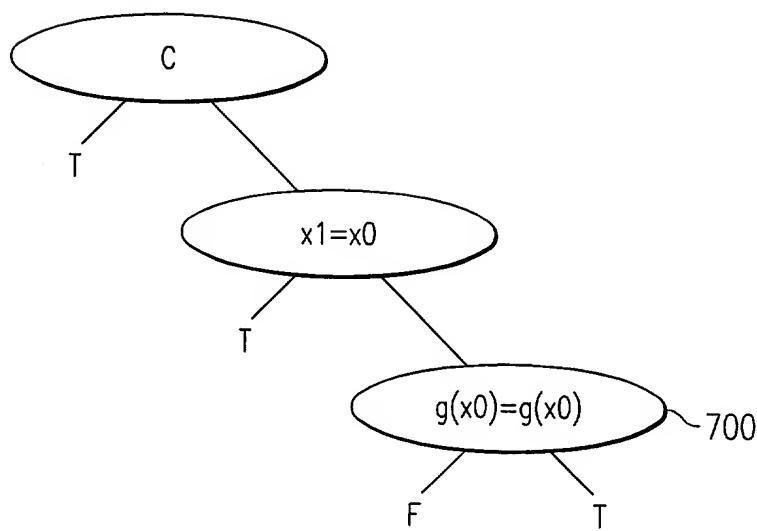


FIG. 7



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FIG. 8

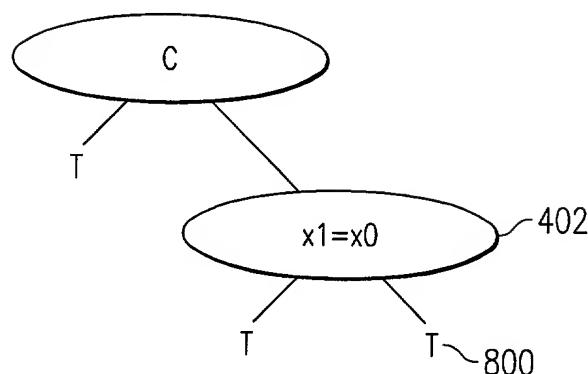


FIG. 9

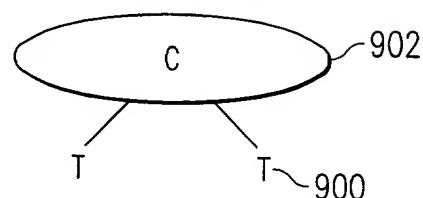
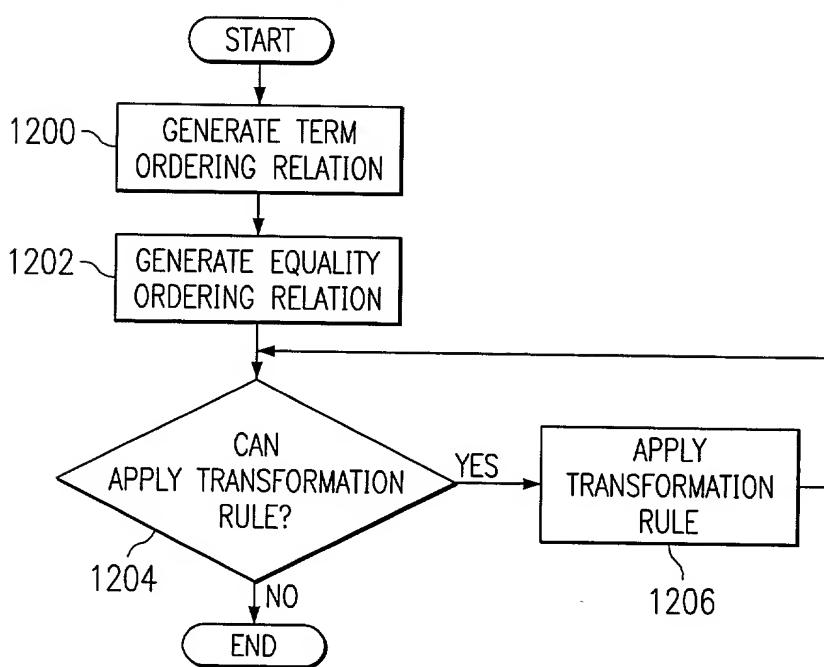


FIG. 10

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FIG. 12



1100

1101 { simplify (X,Y) :- sim (X,Z), !, simplify (Z,Y). FIG. 11
 simplify (X,X).

1102 { sim(ite(S=S, H, _), H).
 sim(ite(S=T, H, K), ite(T=S,H,K)) :-gt(T,S).
 sim(ite(_,H,H), H).
 sim(ite(E, ite(E,H,_), L), ite(E,H,L)).
 sim(ite(E, H, ite(E,_,L)), ite(E,H,L)).
 sim(ite(E1, ite(E2,H,K), L), ite(E2, ite(E1,H,L), ite(E1,K,L))) :-
 gts(E1,E2).
 sim(ite(E1, H, ite(E2,K,L)), ite(E2, ite(E1,H,K), ite(E1,H,L))) :-
 gts(E1,E2).
 sim(ite(S=T, H, K), ite(S=T, L, K)) :-
 gt(S,T), repl(S,T,H,L), H \== L. } 1104

1108 { sim(ite(A,B,C), ite(A,X,C)) :- sim(B,X).
 sim(ite(A,B,C), ite(A,B,X)) :- sim(C,X).

1106 { repl(S,T,S,T) :- !.
 repl(S,T,P,Q) :-
 P = . . [X|Args],
 maprepl(S, T, Args, Newargs),
 Q = . . [X|Newargs].

 maprepl(_, _, [], []).
 maprepl(S, T, [X|A], [Y|B]) :- repl(S,T,X,Y), maprepl (S,T,A,B).

1110 { gts(A=_, C=D) :- gt(A,C), gt(A,D).
 gts(_=B, C=D) :- gt(B,C), gt(B,D).

 depth(P,X) :- atom(P), !, X is 0.
 depth(P,X) :- P = . . [_|Args], max_depth(Args,Y), X is Y+1.

 max_depth([],0).
 max_depth([A|L],X) :- depth(A,Y), max_depth(L,Z), X is max(Y,Z).

1112 { gt(P,Q) :- depth(P,DP), depth(Q,DQ), DP>DQ, !.
 gt(P,Q) :- P = . . [F|_], Q = . . [G|_], F \== G, gtex(F,G), !.
 gt(P,Q) :- P = . . [F|Args1], Q = . . [F|Args2], gtlist(Args1,Args2).

 gtlist([A1|L1],[A2|L2]) :- A1 \== A2, !, gt(A1,A2).
 gtlist([_|L1],[_|L2]) :- gtlist(L1,L2).

1114 { gtex(g,f).
 gtex(x1,x0).